AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Previously presented) A data processor comprising:

one or more functional units arranged to provide an internal processor pipeline,

one or more register files,

a data memory facility having a multibit access port facility,

a snapshot buffer which during handling of an interrupt condition accommodates saving state information of various processor state elements, including state information from the internal processor pipeline, in respective snapshot buffer elements, and

a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility.

2. (Previously Presented) The data processor as claimed in Claim 1, wherein said controller means are arranged to retrieve the saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements upon completing the handling of the actual interrupt condition.

3. (Previously Presented) The data processor as claimed in Claim 2, wherein said controller means are arranged to restore the retrieved saved state information of various processor state elements allowing said data processor to proceed with handling one of an earlier uncompleted interrupt or continuing a main thread of the processing.

4. (Previously Presented) The data processor as claimed in Claim 1, wherein said state information comprise latency data of current operations.

5. (Previously Presented) The data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility.

6. (Previously Presented) The data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility.

7. (Previously Presented) The data processor as claimed in Claim 1, wherein said data memory facility is operated as a stack.

8. (Previously Presented) The data processor as claimed in Claim 7, wherein said stack has a stack pointer that allows multiple stack positions per snapshot.

9. (Previously Presented) The data processor as claimed in Claim 7, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility, and wherein write and read operations in said stack are executed at mutually exclusive instants in time under control of a stack pointer.

10. (Previously Presented) The data processor as claimed in Claim 1, wherein said snapshot buffer is at least substantially constructed from shadow flipflops for storing its snapshot information.

11. (Currently Amended) The data processor as claimed in Claim 1, wherein said snapshot buffer is operated at low power through one or more of clocking shadow flipflops only during actual taking of a snapshot, clocking only the shadow flipflops pointed to by ~~the~~ a stack pointer as a top-of-stack-plus-one during a stack push operation, and clocking the stack pointer itself only during stack pointer updates that are caused by popping and pushing of a snapshot buffer stack.

12. (Previously presented) The data processor as claimed in Claim 1, being a VLIW processor and having a plurality of parallel issue slots of which only a single issue slot is used for implementing handling of nested interrupts.

13. (Previously Presented) A data processing facility comprising the data processor as claimed in claim 1.

14. (Canceled)

15. (Previously Presented) The data processing facility as claimed in Claim 1, wherein the controller means is arranged to save the various processor state elements to the respective snapshot buffer elements in a single clock cycle.

16. (Previously Presented) The data processing facility as claimed in Claim 1, wherein the controller means is arranged to restore the various processor state elements from the respective snapshot buffer elements in a single clock cycle.

17. (Currently amended) The data processing facility of as claimed in Claim 1, wherein the controller means saves, upon occurrence of the subsequent interrupt condition during the handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility without requiring instruction bits, additional to ~~the~~ a stack pointer, for addressing the snapshot buffer elements ~~or the data memory facility~~.